CLAIMS

1. In a cache having a plurality of ways, a method for selecting N ways available for replacement, comprising:

providing a plurality of rulesets, wherein each one of the plurality of rulesets specifies N ways in the cache that are available for replacement, wherein N is an integer equal to or greater than zero;

receiving an access address;

using at least a portion of the access address to select a selected one of the plurality of rulesets; and

using the selected one of the plurality of rulesets, selecting N ways in the cache that are available for replacement.

2. A method as in claim 1, wherein the least a portion of the access address comprises a plurality of contiguous access address bits.

3. A method as in claim 1, further comprising:

providing a first programmable bit to enable replacement of a first one of the plurality of ways.

4. A method as in claim 3, further comprising:

providing a second programmable bit to enable replacement of a second one of the plurality of ways.

5. A method as in claim 4, wherein a first one of the plurality of rulesets comprises the first and second programmable bits.

6. A method as in claim 5, further comprising:

providing a third programmable bit to enable replacement of the first one of the plurality of ways; and

providing a fourth programmable bit to enable replacement of the second one of the plurality of ways,

wherein a second one of the plurality of rulesets comprises the third and fourth programmable bits.

7. A method as in claim 1, wherein the at least a portion of the access address comprises a plurality of bits, and wherein the plurality of bits comprises a highest order bit of the access address.

8. A method as in claim 1, wherein the at least a portion of the access address has no further use in the cache.

9. A method as in claim 1, further comprising:

selecting a plurality of bits of the access address to use as the at least a portion of the access address.

10. A method as in claim 1, further comprising:

decoding the at least a portion of the access address, wherein said step of decoding is performed before said step of using at least a portion of the access address to select a selected one of the plurality of rulesets.

11. A method as in claim 1, further comprising:

providing a ruleset selection control register which receives the at least a portion of the access address and which provides a ruleset indicator for selecting at least one of the plurality of rulesets.

12. A method as in claim 1, further comprising:

providing a first address range corresponding to a first one of the plurality of rulesets; and

determining if the access address is within the first address range.

13. A method as in claim 12, further comprising:

providing a second address range corresponding to a second one of the plurality of rulesets; and

determining if the access address is within the second address range.

14. A method as in claim 13, further comprising:

if the access address is not within the first address range and is not within the second address range, using a default ruleset from the plurality of rulesets.

15. A method as in claim 1, wherein the cache is formed as a portion of an integrated circuit.

16. An integrated circuit comprising a cache having a plurality of ways, the cache comprising:

ruleset selection circuitry comprising ruleset storage circuitry for storing a plurality of rulesets, wherein each one of the plurality of rulesets

specifies N ways in the cache that are available for replacement, wherein N is an integer equal to or greater than zero, the ruleset selection circuitry uses at least a portion of an access address to provide at least one selected ruleset signal; and

replacement control circuitry, coupled to the ruleset selection circuitry to receive the at least one selected ruleset signal, the replacement control circuitry uses the at least one selected ruleset signal to select N ways in the cache that are available for replacement.

17. An integrated circuit as in claim 16, wherein the ruleset selection circuitry further comprises:

first storage circuitry for storing one of a base address value and a lower bound value; and

second storage circuitry for storing one of a mask value and an upper bound value.

18. Cache control circuitry, comprising:

storage circuitry for storing a plurality of rulesets;

circuitry coupled to said storage circuitry, wherein said circuitry uses a portion of an access address to generate a ruleset indicator, said ruleset indicator being used to select at least one of the plurality of rulesets, and

wherein said one of the plurality of rulesets is used to select at least zero or more ways in the cache that are available for replacement.

19. The cache control circuitry of claim 18, wherein said storage circuitry comprises at least one user programmable control register.